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ASTIA 274054
CATALOGUE NO. AS AD INC.

274054

Improved Phase Modulator-Demodulator

Report No. 2

Contract No. DA-36-039-SC 87248

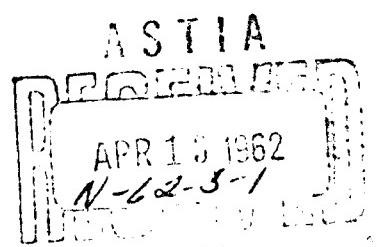
Second Quarterly Progress Report

1 September 1961 to 30 November 1961

U. S. Army Signal Research and Development

Laboratory

Fort Monmouth, New Jersey



459450

Federal Systems Division
INTERNATIONAL BUSINESS MACHINES CORPORATION
ROCKVILLE, MARYLAND

Improved Phase Modulator-Demodulator

Report No. 2

Contract No. DA-36-039-SC 87248

SIGNAL CORPS TECHNICAL REQUIREMENT

SCL- 4269

5 SEPTEMBER 1960

**Second Quarterly Progress Report
1 September 1961 to 30 November 1961**

Objective

***To provide two development models
of a phase modulator-demodulator.***

PREPARED BY

Margaret George

CONTENTS

		Page
Section 1	STATEMENT OF PURPOSE	1
Section 2	ABSTRACT	2
Section 3	PUBLICATIONS, LECTURES, REPORTS AND CONFERENCES	3
Section 4	FACTUAL DATA	5
4.1	Electrical Design	5
4.1.1	Logic Design	5
4.1.2	Circuit Design	9
4.1.3	Miscellaneous Electrical Parts	18
4.1.4	Card Layout and Drawings	18
4.2	Mechanical Design	18
Section 5	CONCLUSIONS	20
Section 6	PROGRAM FOR NEXT REPORT INTERVAL	21
6.1	Electrical Design	21
6.2	Mechanical Design	21
Section 7	KEY TECHNICAL PERSONNEL	22
Section 8	ABSTRACT CARDS (ASTIA)	24
Section 9	DISTRIBUTION LIST	25

ILLUSTRATIONS

Figure		Page
1	Input Conversion and Transmitter Logic	7
2	Input Conversion and Transmitter Timing	8
3	Receiver and Output Conversion Logic	10
4	Receiver and Output Conversion Timing	11
5	Data (or Ready) Input Converter	12
6	Strobe Input Converter	13
7	Transmitter Phase Modulator	15
8	Receiver Amplifier	16
9	Rectifier	17

Section 1

STATEMENT OF PURPOSE

The purpose of this contract is to design and build two developmental modulator-demodulator units. Provision is to be made for conversion from parallel FIELDATA information to serial information for transmission over a telephone line and for conversion back to parallel FIELDATA information in the receiver. Provision for character framing is to be included. The work is broken down into the following areas:

1. Logic and circuit design.
2. Mechanical design.
3. Power supply procurement or design.
4. Parts procurement.
5. Manufacturing and test.
6. Environmental test.
7. Final reports.

Work on the basic circuits to be used is being done by a group on another project. These circuits will be used in the input and output conversion sections of the logic.

Section 2

A B S T R A C T

This report describes the progress made in the design of a modulator-demodulator. The logic, circuit, and mechanical designs of the units are covered in detail. The sync bit problem is described and its solution discussed. Although this problem has caused considerable difficulty in the last quarter and most of the effort has been spent on it, some progress on the special circuits has also been made. The one major area that may cause problems is the question of the reliability of the basic circuits at 0°C. The details of this problem are also discussed in this report.

Section 3

PUBLICATIONS, LECTURES, REPORTS, AND CONFERENCES

No publications, lectures, or reports have resulted from work under this contract during the report period. The following list condenses the results of conference, group discussion, or consultation involving IBM personnel and representatives of the procuring agency.

1. On 11 September 1961 a meeting was held at Ft. Monmouth to discuss the progress that had been made and some of the mechanical design requirements. Those present included J. Stout, Signal Corps; M. A. George, H. Baas, L. E. Moser, and A. G. Stritt, of IBM. Several other Signal Corps personnel were also present during that part of the meeting when certain aspects of the job were discussed in detail. The progress described in the first quarterly report was reviewed. Many mechanical details were discussed. It was agreed that the connectors could be located in the front of the unit rather than in the back. The units will be operated in the transit case, so that provision for adequate cooling must be included in the design. The maximum dimensions of the units were also discussed.

2. A meeting was held at Ft. Monmouth on 13 October 1961 to discuss the transfer of the contract from IBM Kingston to the IBM Communications Systems Center in Rockville, Maryland. Those present were Major Vogel, J. Stout, R. McMurray, and T. Calafato of Ft. Monmouth and R. Ballance, R. Brainard, G. Bruno, and J. Puente of IBM. No legal problem in the transfer of the contract was foreseen. It was agreed that the contract would not be changed in any manner and that the engineer responsible for the project would also be transferred.

3. A telephone conversation was held between J. Stout and M. A. George on 2 November 1961. It was determined that an all-zeros pattern

is a legitimate character, so that an all-zeros pattern cannot be used to indicate the absence of data. J. Stout stated that he and R. Tucker were planning to visit the Communications Systems Center late in November. Further details would be arranged later.

4. On 15 November 1961 another telephone conversation was held between J. Stout and M. A. George. J. Stout suggested that, if necessary, a switch could be used to distinguish between continuous and intermittent operation. If the input data is always available when the transmitter is ready to transmit, then no indication of no data is needed. If the input data is intermittent or slower than the transmitter, then an indication that a particular character is not data is needed. In this case, an all-zeros pattern could be used to indicate the absence of data. The switch would be used to select one of these two types of operation. The disadvantage of this system is that an all-zeros pattern is still a legal character, so that in the slow-speed position of the switch, the output data would not contain any character that was all zeros even though the input data contained this character. M. George stated that an alternate method of indicating the absence of data had been devised.

J. Stout stated that, unless someone was planning to be gone on 28 November, he and R. Tucker were planning to be here to observe what has been done. The details of that meeting will be covered in the next quarterly report.

Section 4

F A C T U A L D A T A

4.1 Electrical Design

4.1.1 Logic Design

In the original proposal, it was decided to have 8 data bits and one sync bit of about twice the data amplitude for each character. As the design work progressed, it became obvious that a 2 to 1 ratio was not going to be high enough because of the DC component in the signal and because of the way the signal would be distorted when it is passed over the telephone line. Because this distortion could be very great, it was estimated that a 6 to 1 ratio would be required. Since the maximum signal amplitude that the telephone system can tolerate is +5 dbm, it would be necessary to set the maximum sync amplitude at +5 dbm and the maximum data amplitude 16 db below it or -11 dbm. This also means that the minimum input to the receiver would be -36 dbm for the sync pulse and -52 dbm for the data. Because this level is so low that noise would be a problem, a better means of generating a sync pulse was investigated.

The first method investigated was to modulate the output signal with the filtered data signal. This method eliminates the DC component caused by using 1 1/2 cycles per bit. However, the phone-line distortion is great enough that the sync-to-data ratio would still be high.

Since amplitude modulation did not seem practical, several methods of using a different frequency signal to indicate sync were then investigated. Each of these methods had the disadvantage of having the data

frequencies delayed by the phone line by amounts different from the sync frequency, so that correct timing would be difficult to establish. These methods also added to the complexity of the transmitter and receiver.

At this point it was decided that amplitude modulation was a poor solution and that because of the phone-line delay distortion the sync signal should contain the same frequency components as the data. If a greater length of time were available for the sync bit, a phase shift could be produced in the center of a bit to indicate sync. A time equal to three data bit lengths would be required in order that the frequency components produced not be too high. This method would result in the fewest changes to the logic and circuits. A disadvantage is that only 8 out of 11 bits would be used for data; however, keeping the logic in sync is important enough that the use of 3 bits out of 11 seems justified. In addition, a carrier frequency of 1650 cps could be used so that there would be one cycle per bit.

The logic needed to detect this sync bit was investigated. It was determined that it is necessary to shift phase at the beginning of the 3 sync bits as well as in the center in order to detect the shift in the center. If this is done, it is no longer possible to use a shift at the beginning of the sync bit to indicate no data. Therefore, another method of indicating whether the transmitter character is real data was needed. If an all-zeros pattern were an illegal character, this pattern could be used to indicate no data. However, an all-zeros character is legal. If an input buffer register is used, then a special character can be sent with a shift in the middle of one of the bits to indicate no data. In studying the logic required to detect this signal, the easiest character to detect is one with a shift at the beginning of the first bit and a shift in the middle of the second bit.

The changes required in the input conversion and transmitter logic were slight. An input buffer was added and the oscillator changed to 1650 cps. An extra counter stage for 150 bits per second was added. The logic and timing drawings are shown in Figures 1 and 2.

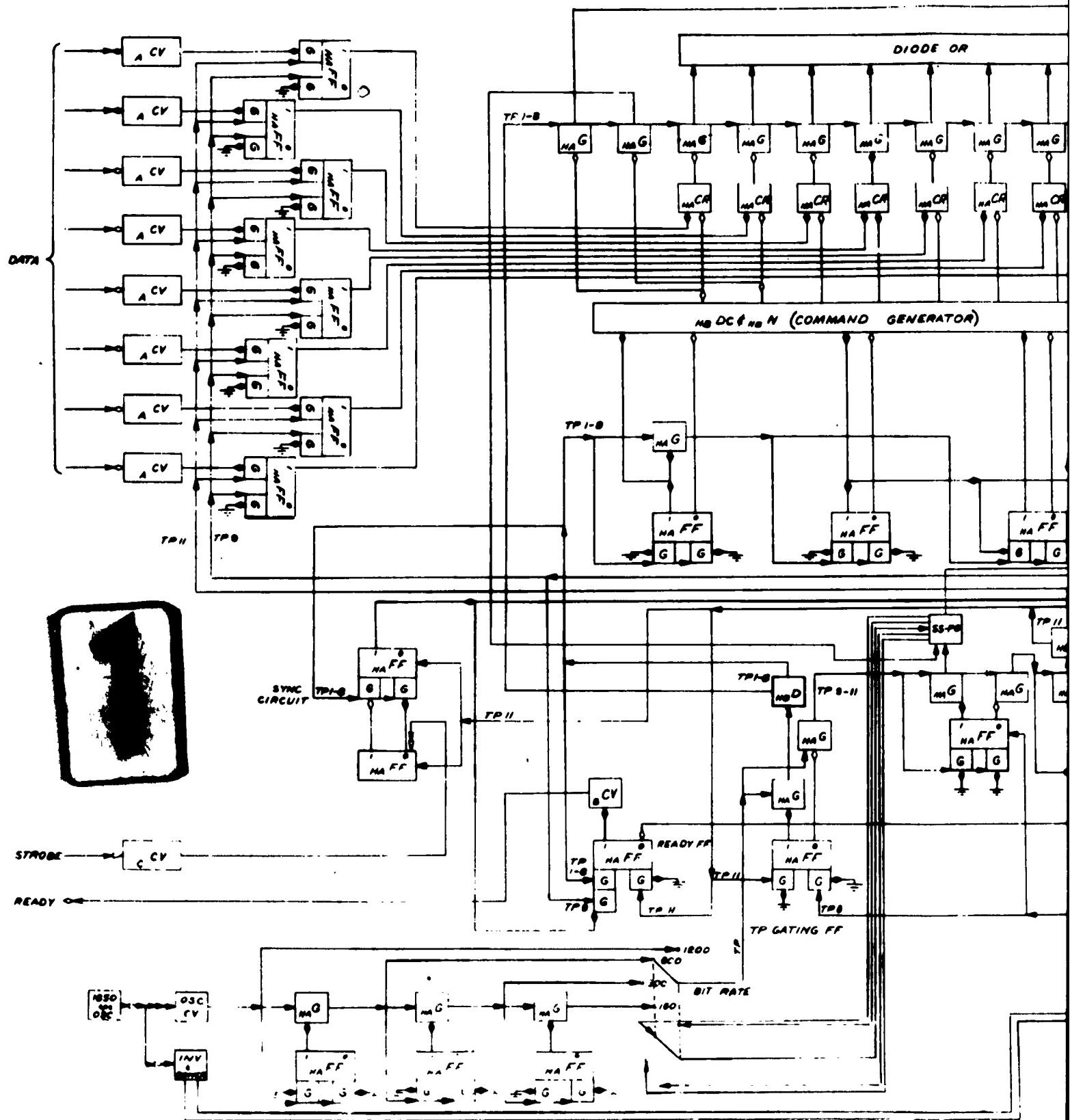
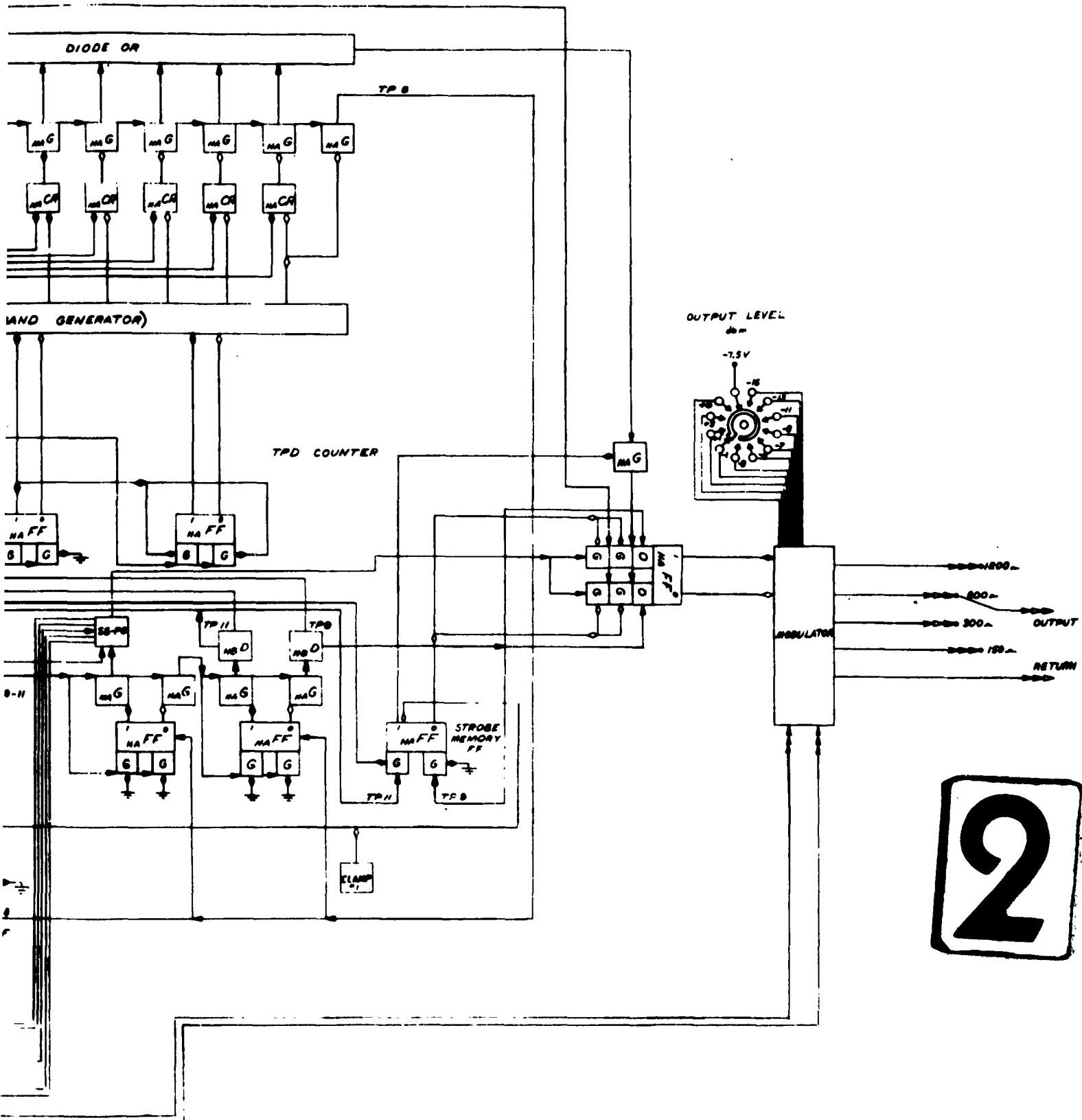


Figure 1. Input Conversion and Trans-

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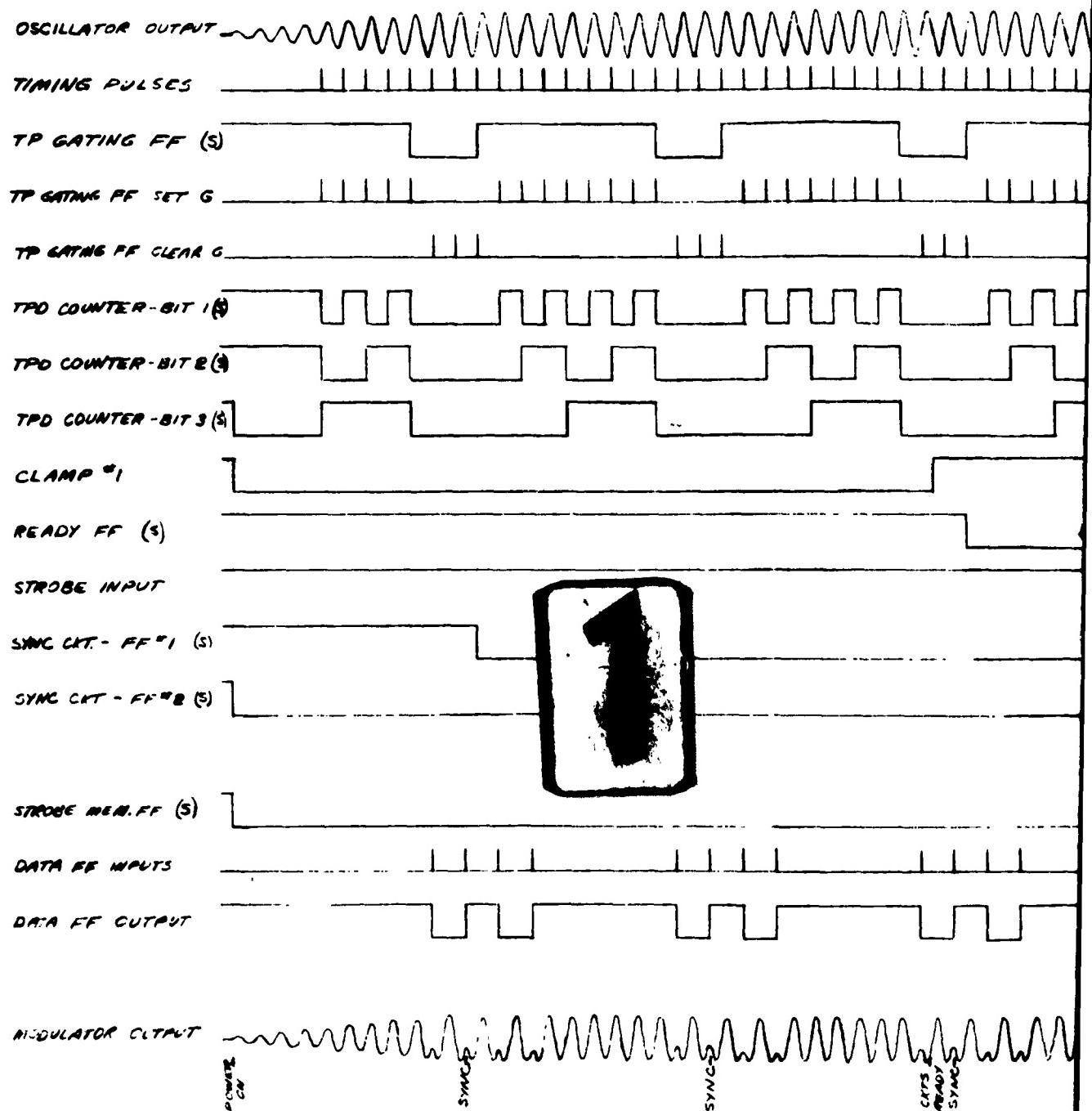
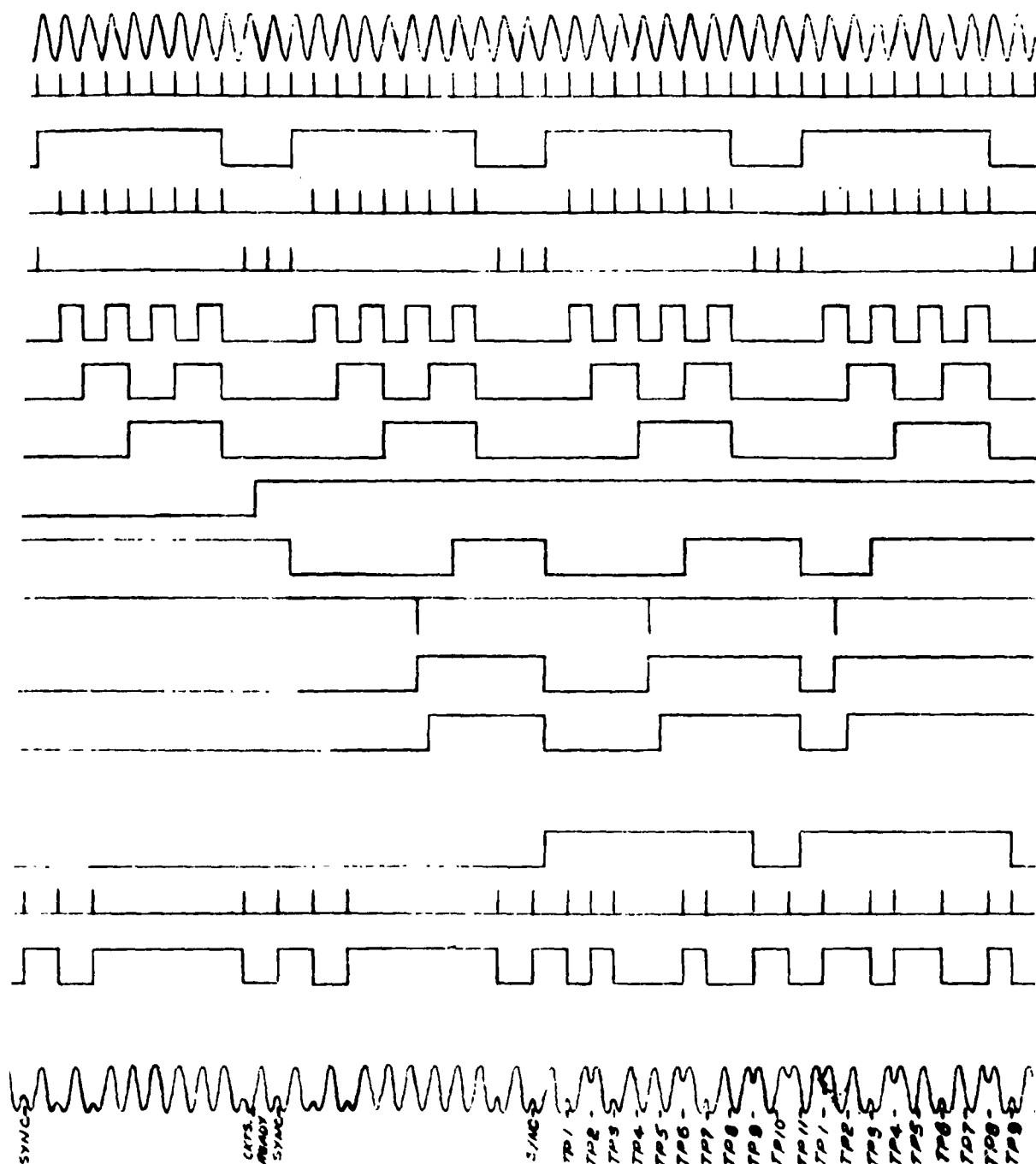


Figure 2. Input Conversion and Transmitter Tim

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It was determined that, in the receiver, a later demodulation scheme developed by IBM would cause fewer timing problems and would require less space than the demodulation scheme originally proposed. Also, because of frequency translation, it is not practical to derive timing pulses from the recovered carrier frequency. It is necessary to use an accurate oscillator at 1650 cps and to sync it with the data pulses. These changes were made in the receiver logic. Drawings of the logic and timing charts are shown in Figures 3 and 4.

The problem of having enough space in the units to accommodate all the cards, power supplies, and large components still exists. The problem has been aggravated by the addition of the input buffer and extra counter stages for 150 bits per second operation. The logic and the circuits are being simplified as much as possible in order to reduce the space required. The real question—the answer to which is not yet known—is how large the power supplies have to be. It is still thought to be possible to fit all the equipment in one tray.

4.1.2 Circuit Design

- (a) Data (or Ready) Input Converter (_A CV in logic diagram). The design of this circuit is complete, and card layout has been started. A schematic is shown in Figure 5.
- (b) Strobe Input Converter (_C CV in diagram). This circuit is similar to the Data Input converter. The design is complete, and card layout has been started. A schematic is shown in Figure 6.
- (c) Data (or Ready) Output Converter (_B CV in diagrams). The design was completed last quarter, and card layout has started.
- (d) Strobe Output Converter (_D CV in diagram). Nothing new to report except that card layout has been started.
- (e) 1650 cps Oscillator (Transmitter). The logic changes have necessitated a change in frequency and a tighter tolerance on frequency. Otherwise the situation is the same as reported last quarter.
- (f) Oscillator Converter. Some modifications to an existing circuit are required.

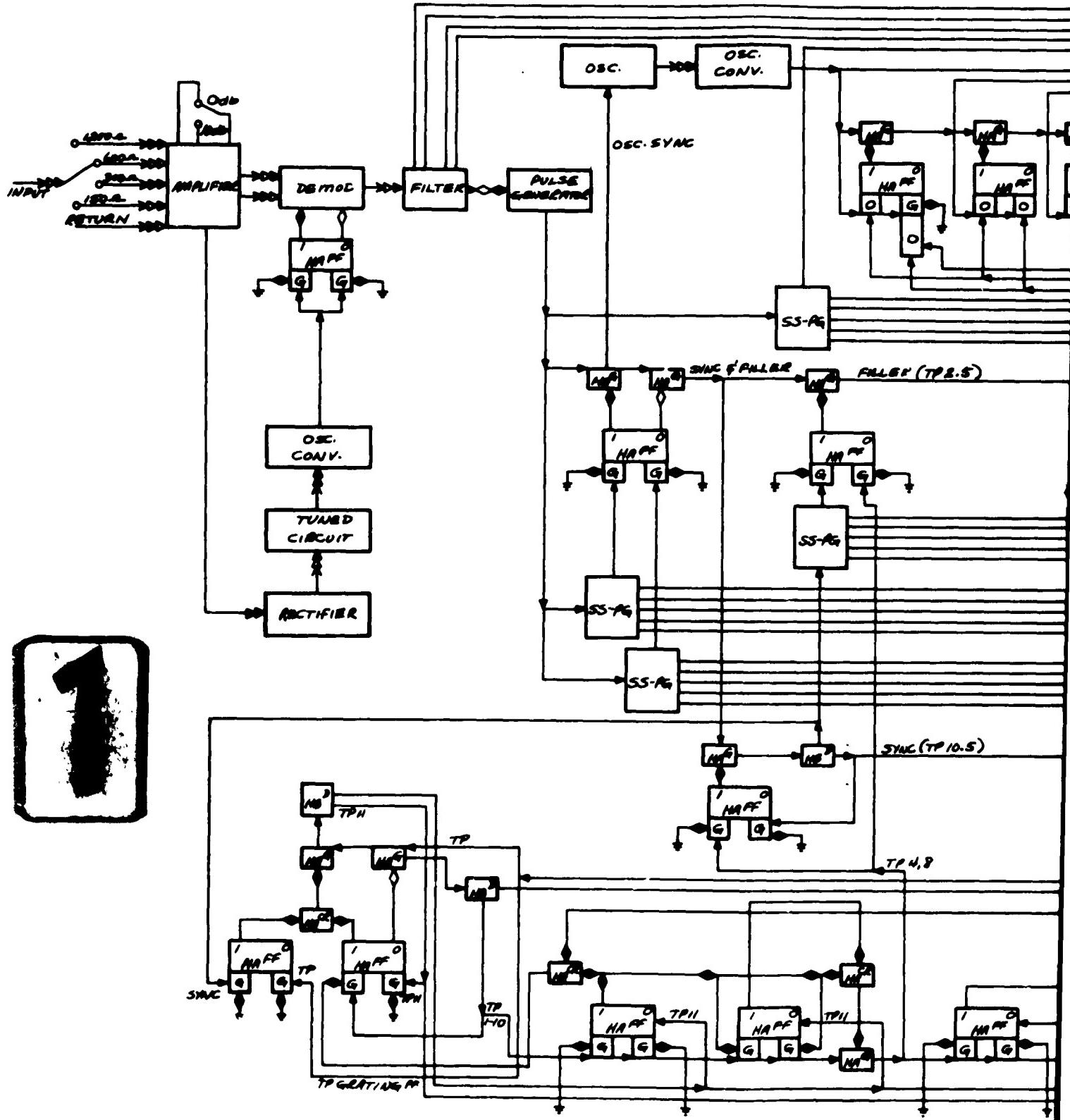
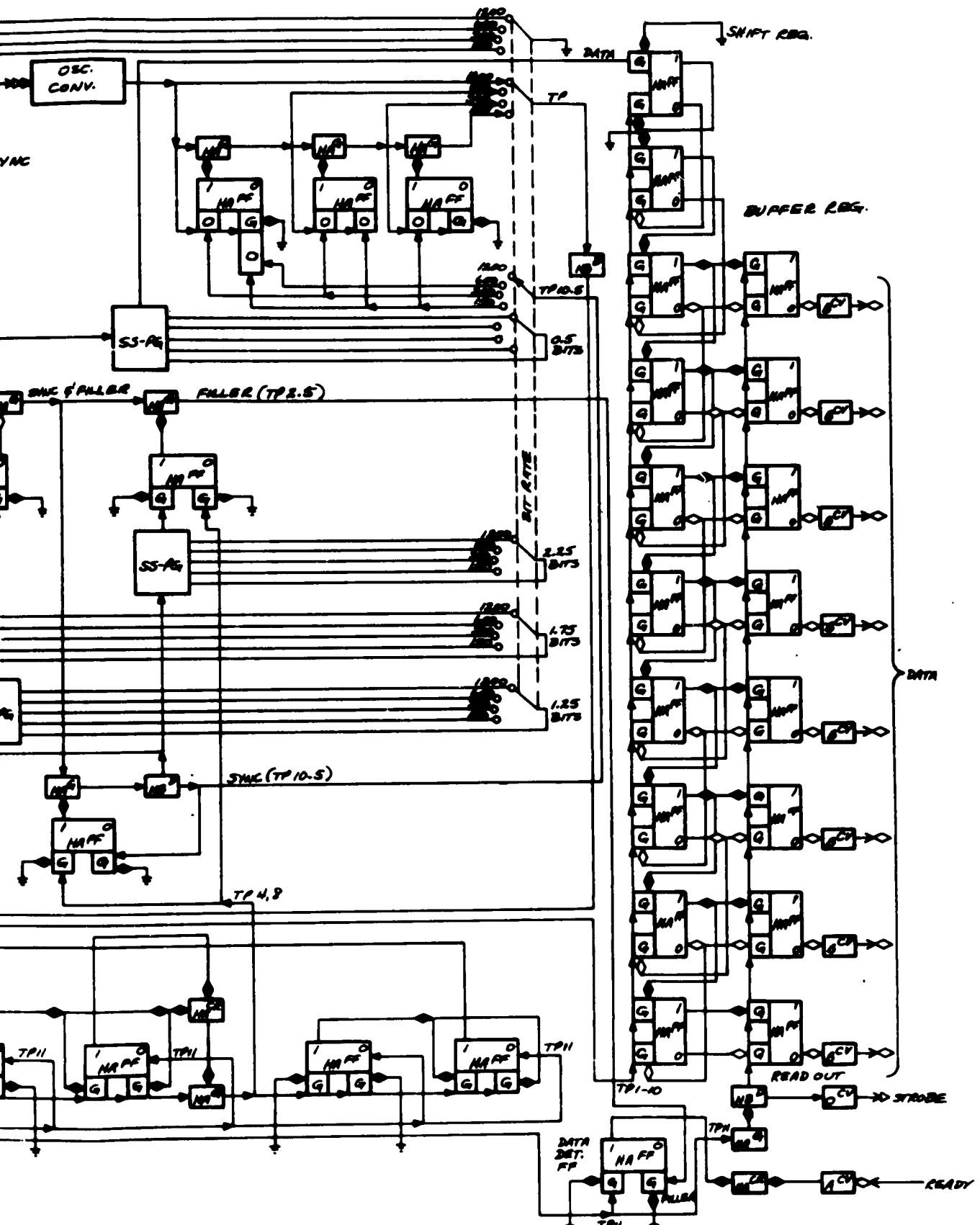


Figure 3. Receiver and Output Conversion Logic



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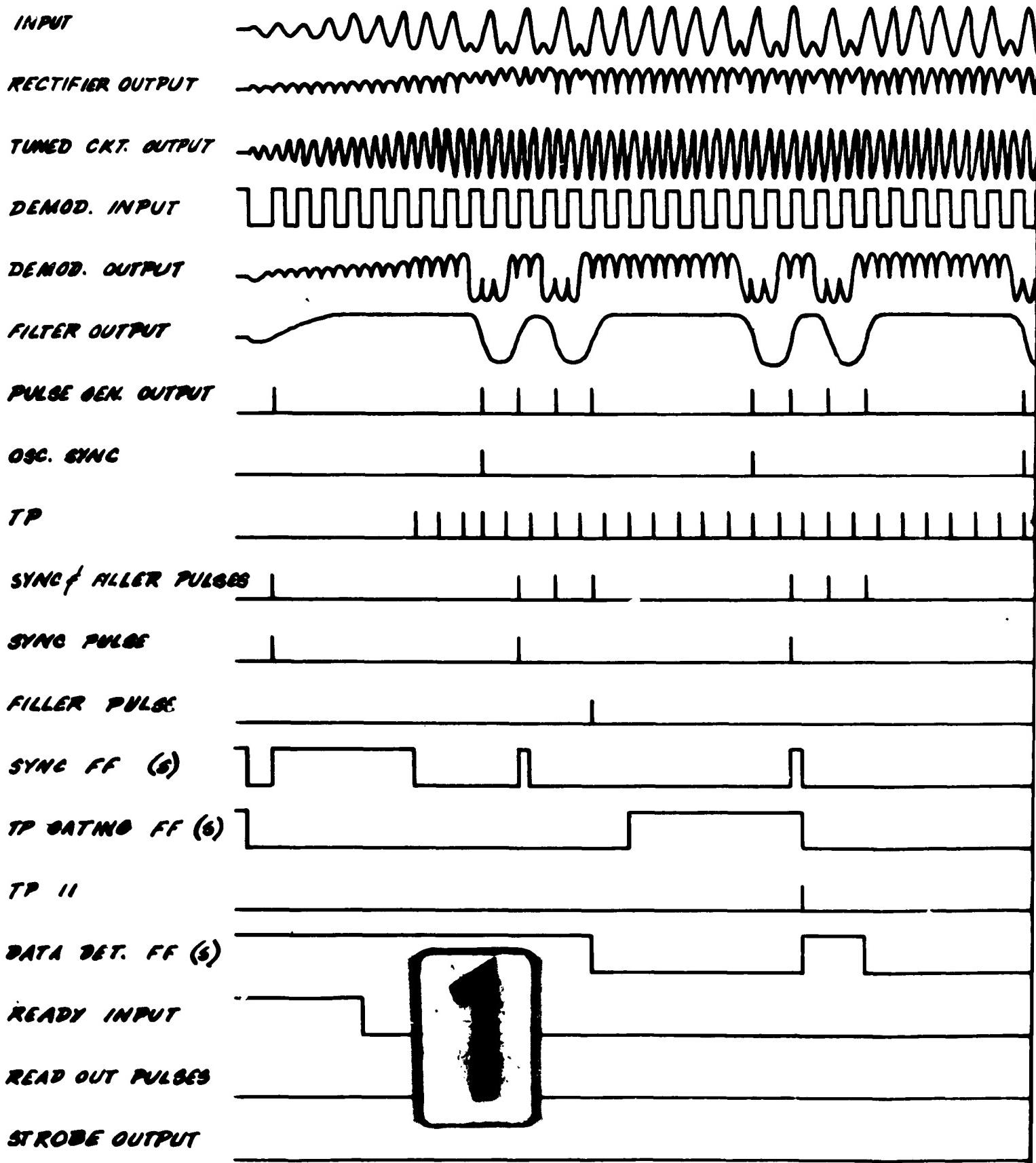
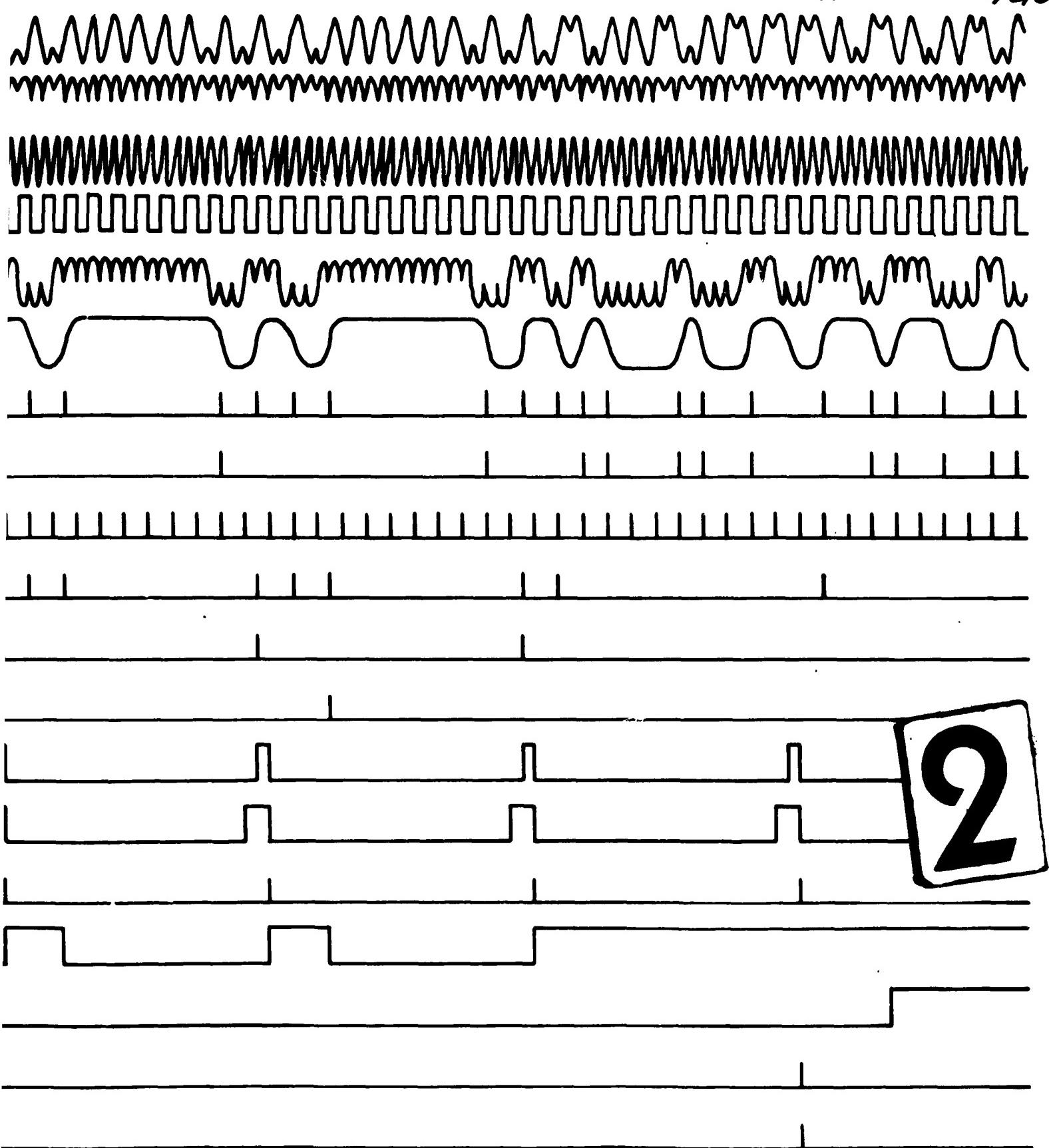


Figure 4. Receiver and Output Con

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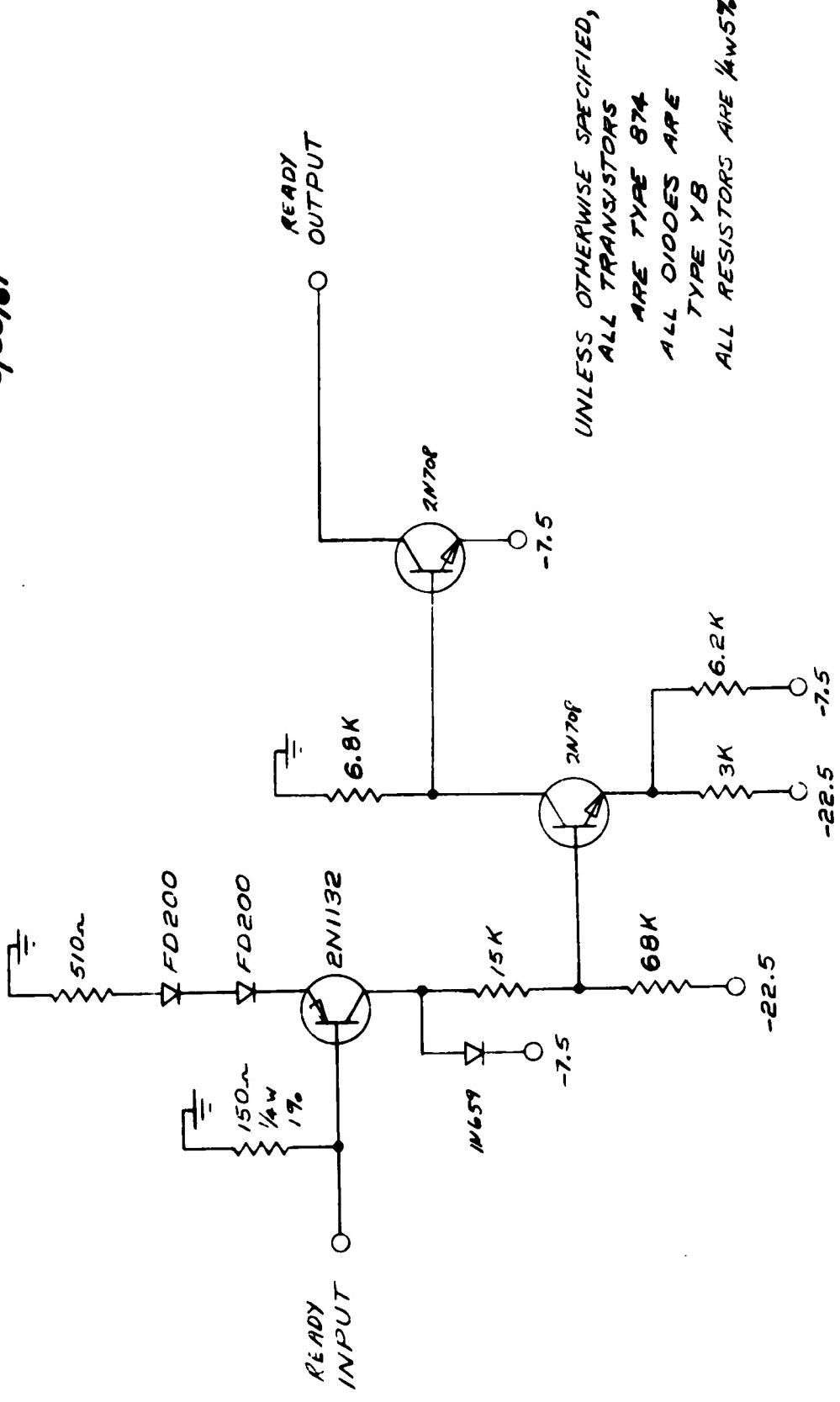


Figure 5. Data (or Ready) Input Converter

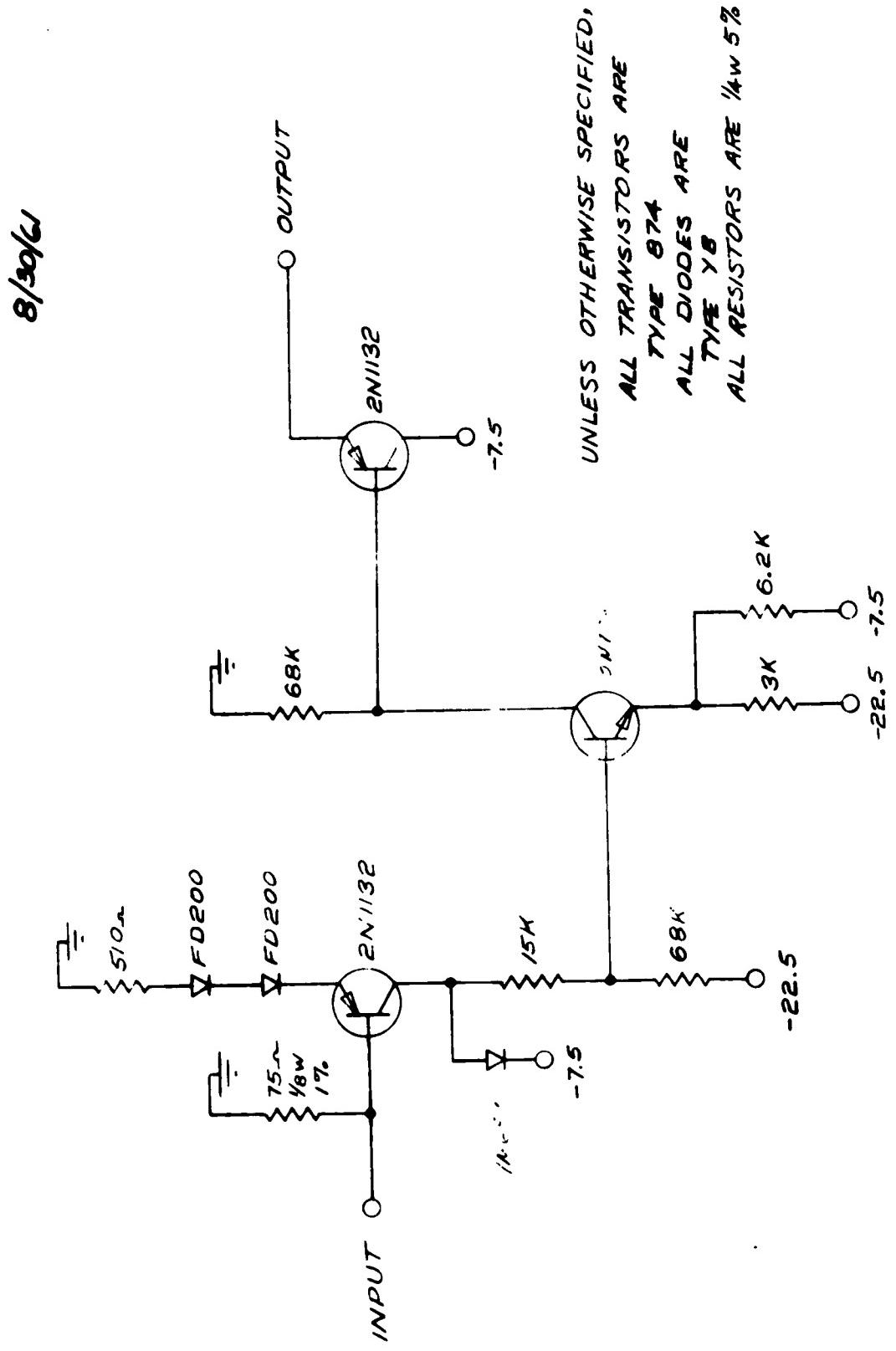


Figure 6. Strobe Input Converter

- (g) Transmitter Phase Inverter. Nothing new to report.
- (h) Transmitter Phase Modulator. This circuit has been modified because of the new modulation method being used. The sync section has been removed, a low pass filter has been added, and the driver stages have been simplified. Further testing in the lab is required. A schematic is shown in Figure 7.
- (i) Clamps. One of these circuits has been eliminated. Otherwise, there is nothing new to report.
- (j) Single Shot - Pulse Generator. Nothing new to report.
- (k) Diode OR. Nothing new to report.
- (l) Receiver Amplifier. The dynamic range of the amplifier has been increased. It is possible that the 10 db attenuator may not be needed. The stability has also been greatly improved. Other improvements in the circuit have also been made. Further testing is required to make sure that the circuit will operate properly as components, power supply voltages, and temperature are varied. Refer to Figure 8 for a schematic.
- (m) Rectifier. This circuit has been designed. Some further testing is required. A schematic is shown in Figure 9.
- (n) Tuned Circuit. Some of the design and testing of this circuit has been done. At 90° phase shifting circuit must be incorporated into the present design.
- (o) Demodulator. This circuit is the same as the modulator gating circuit. Some additional emitter follower stages may be required to drive its load.
- (p) Filter. Work has not started on this circuit.
- (q) Pulse Generator. Nothing new to report.
- (r) Oscillator (Receiver). This oscillator must operate at 1650 cps but be kept in synchronism with the data. Several vendors have been contacted concerning the possibility of designing this oscillator.
- (s) Previously Developed IBM Circuits. Some difficulty has been experienced in getting these circuits to operate reliably at 0°C under worst conditions of components and voltage variations. The seriousness

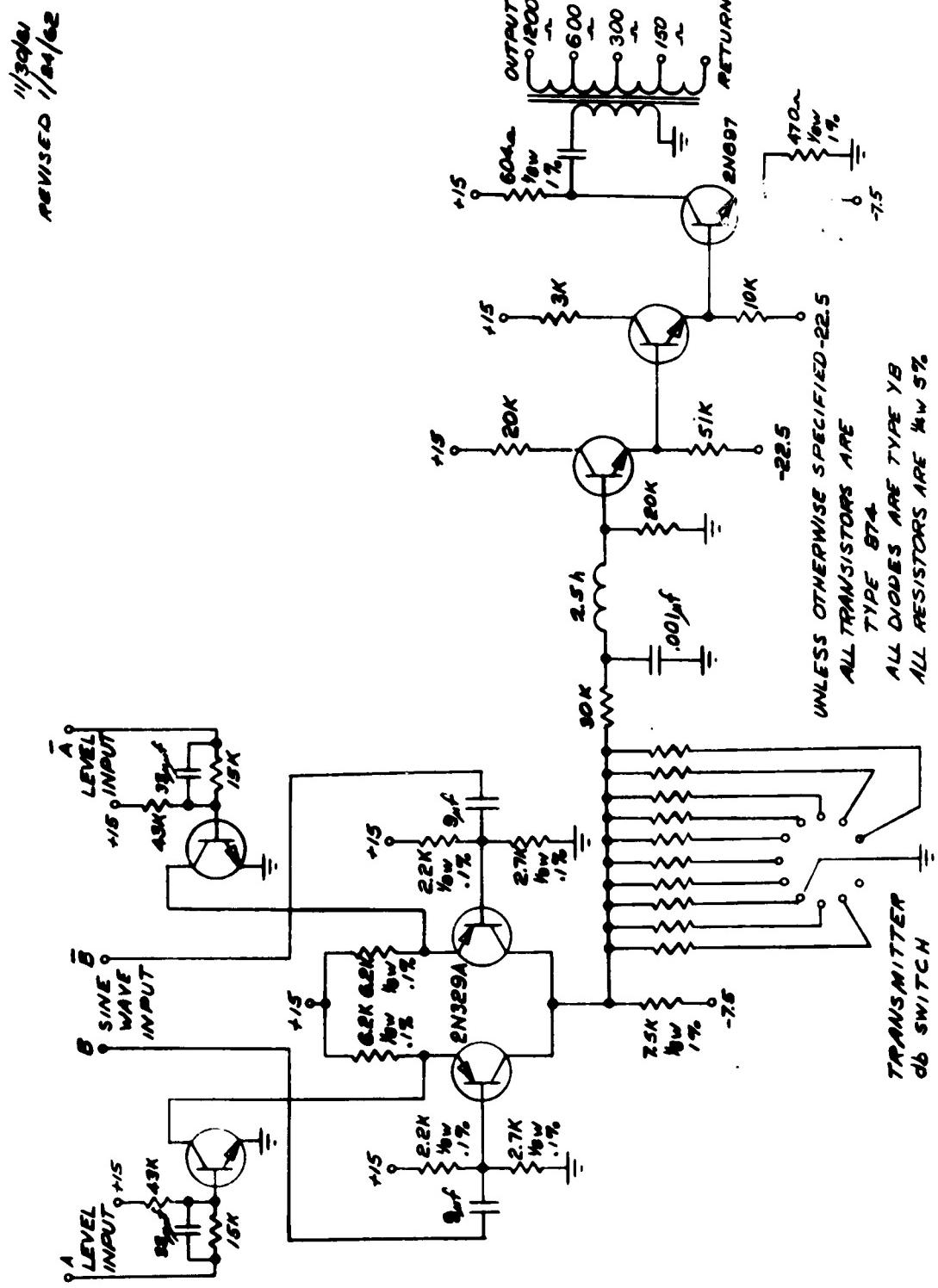
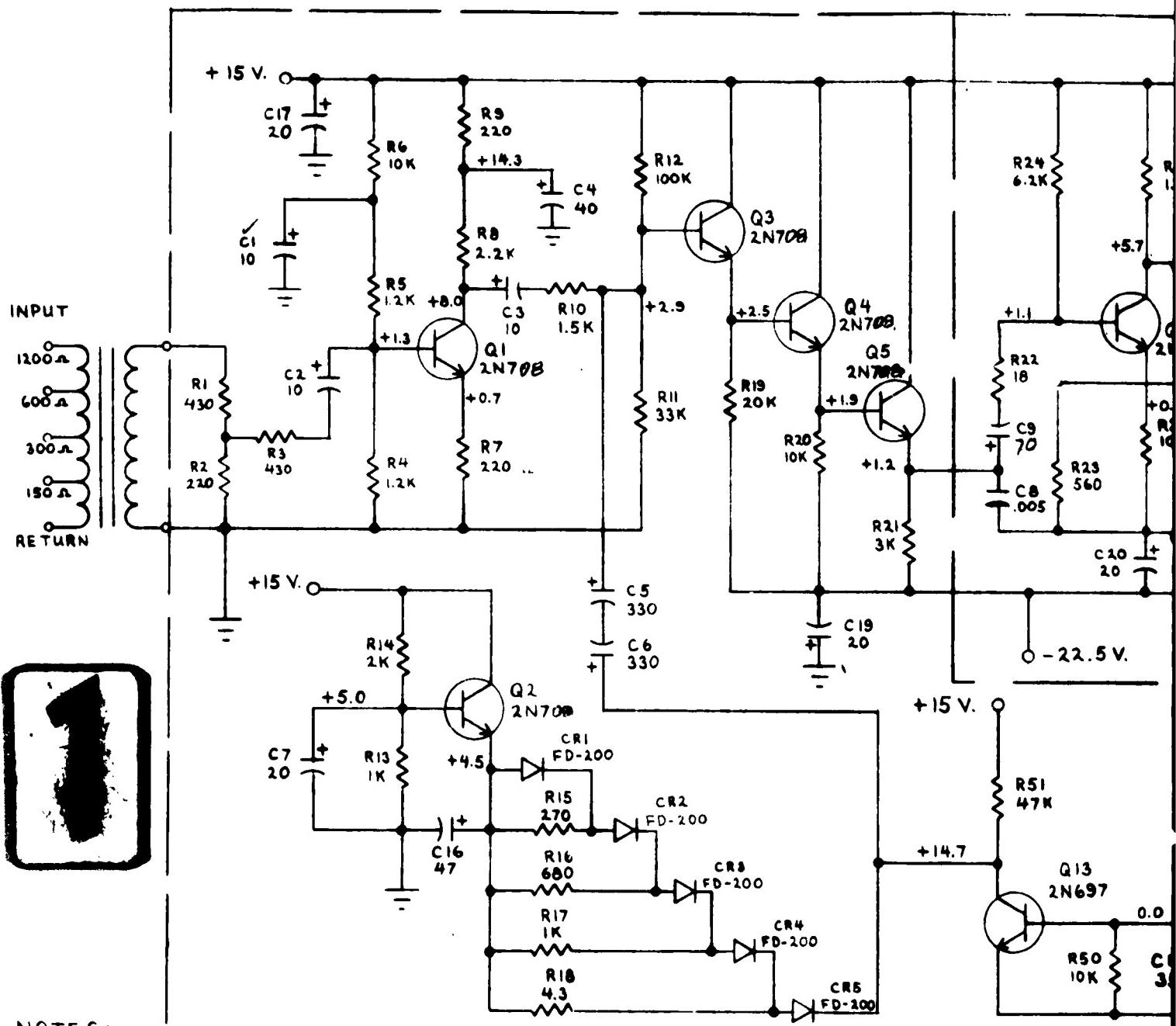


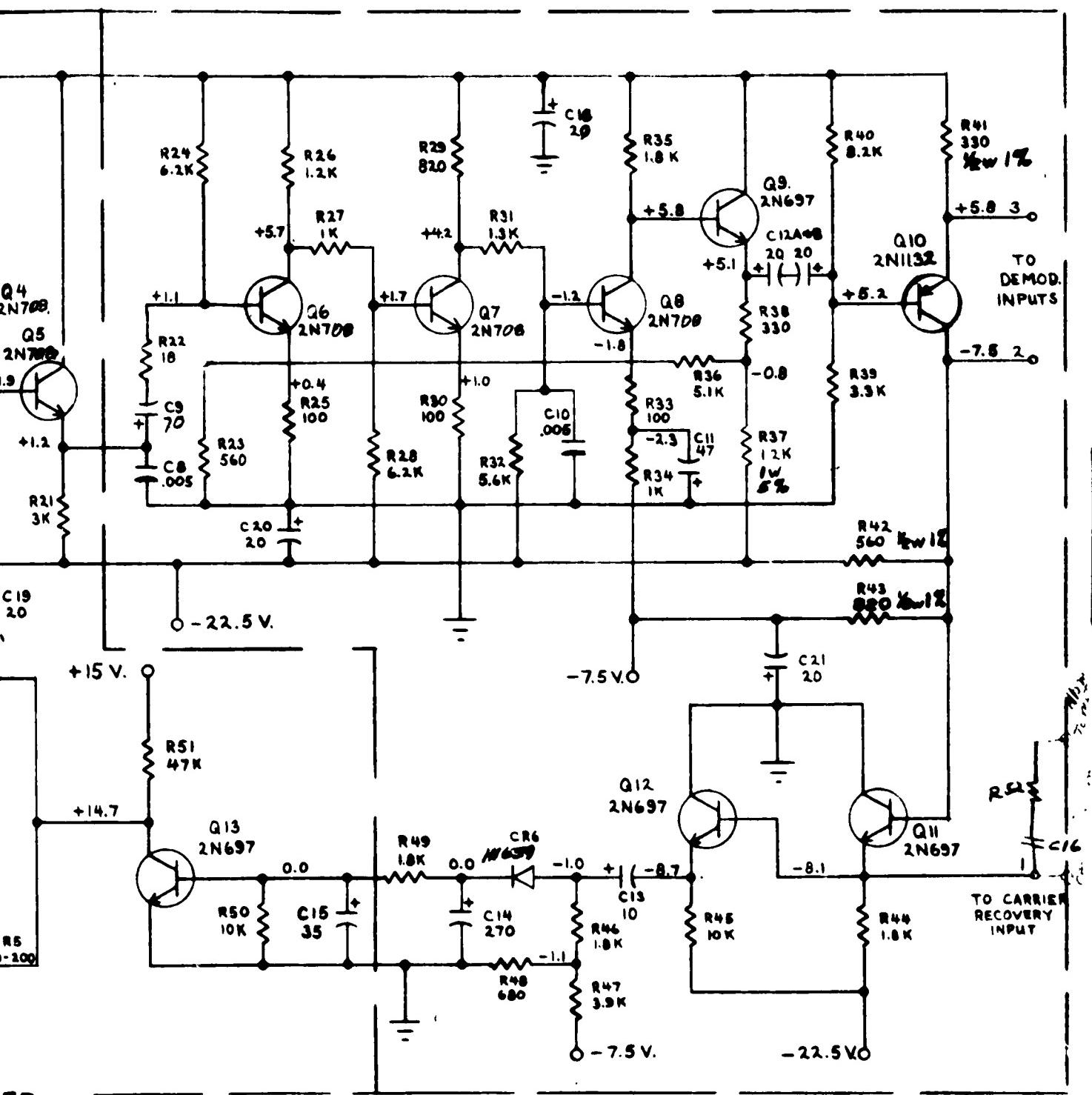
Figure 7. Transmitter Phase Modulator



NOTES:

1. ALL CAPACITORS IN UF, ALL RESISTORS IN OHMS.
- 2 VOLTAGES MEASURED WITH 20K Ω/V METER
WITH INPUT SIGNAL OFF.
3. ALL RESISTORS ARE ± 5% UNLESS OTHERWISE SPECIFIED
4. 1% RESISTORS ARE METAL FILM.

Figure 8. Receiver Amplifier



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Figure 8. Receiver Amplifier

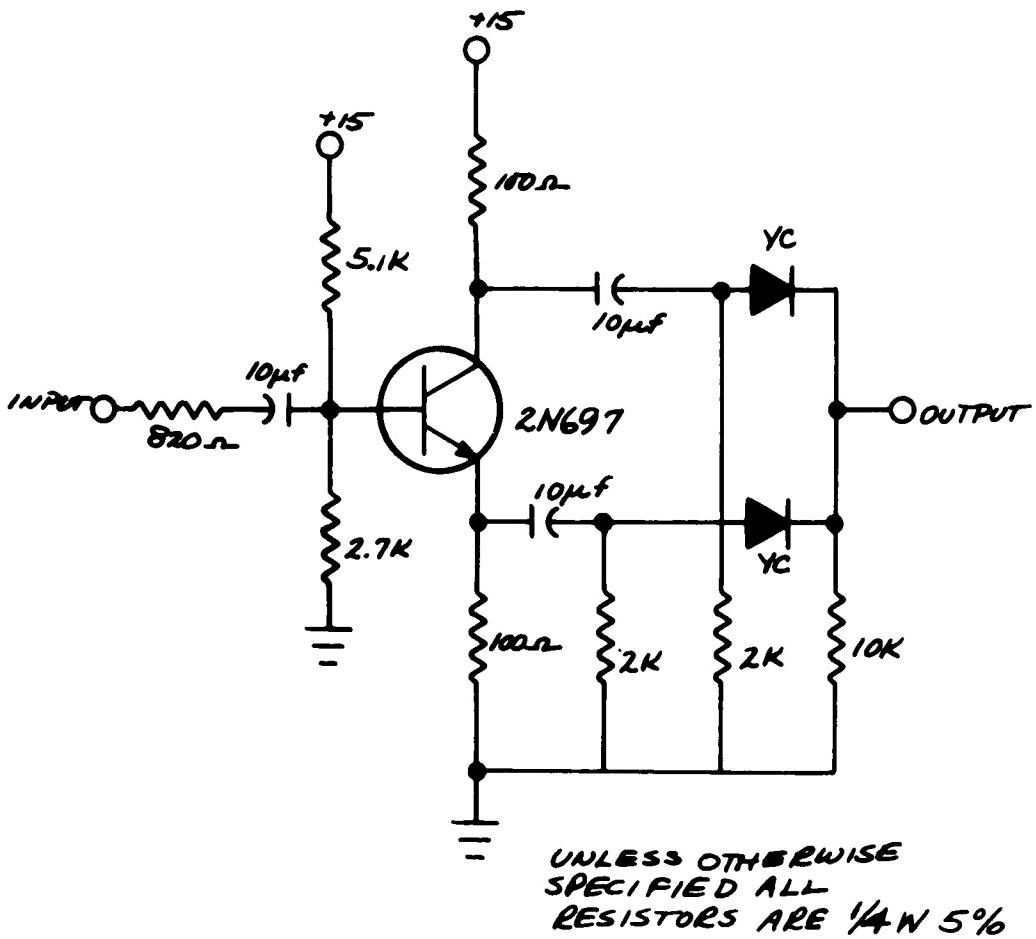


Figure 9. Rectifier

of this problem is not known exactly. An attempt is being made to modify the circuits so that they will work down to -40° C. It now appears that extensive modifications in the circuits will be necessary to meet this low temperature requirement. One of the power supply voltages will probably have to be changed or the driving ability of the circuits reduced considerably. In either case, extensive modifications will be required in the special circuits or logic. Also, these circuits may not be designed in time to meet the schedule. Therefore, a thorough investigation of the reliability of the original circuits at 0° C is planned. A decision will then be made as to whether these circuits can be used.

4.1.3 Miscellaneous Electrical Parts

- (a) I/O Transformers. Nothing new to report.
- (b) db Meter. All the problems of getting a meter to meet the requirements have been solved. Two meters have been ordered.
- (c) Miscellaneous Inductors and Filters. Standard off-the-shelf units will be used if possible. Some sample inductors have been ordered.
- (d) Miscellaneous Switches. Nothing has been done.
- (e) Power Supplies. Stock units that will meet the electrical mil spec and space requirements cannot be obtained. Special power supplies will have to be designed. A decision is still pending on whether to design the power supplies ourselves or to have a vendor do it for us.
- (f) Mechanical Components. Most of the standard mechanical parts have been ordered and received.

4.1.4 Card Layout and Drawings

Very little work has been done in this area. As each circuit becomes definite, this work will continue.

4.2 Mechanical Design

Very little work can be done on the mechanical design of the unit until the dimensions of all the parts to be used are known. The approximate

number of cards required has been determined. The physical dimensions of the inductors, transformers, filters, and power supplies are not yet known. As soon as these dimensions are established, the mechanical design work will be resumed.

Section 5

CONCLUSIONS

The problem of obtaining a good method of generating and detecting a sync bit has resulted in a considerable amount of logic and circuit redesign. However, it is felt that this method, which uses a phase shift in the center of a bit, is the best and simplest method to use in a unit of this small physical size. Although there is some question of the reliability of detecting this sync bit if a poor telephone line is used, no problem should result over a reasonably good line.

Most of the effort in this quarter has been devoted to finding a solution to the sync problem; additional design work has also been done on some of the circuits. The only circuit that is likely to cause any real problems is the oscillator, which must be kept in sync with the data.

The basic circuits to be used are still in doubt. Whether the circuits as they presently exist will be satisfactory is not known. If they are not, it may be some time before the new circuits are designed. In addition, use of the new circuits may mean some redesign of the special circuits for the transmitter and receiver. A decision will be made within the next two weeks concerning which circuits to use.

Section 6

PROGRAM FOR NEXT REPORT INTERVAL

6.1 Electrical Design

- 1. Complete the design and testing of all circuits.**
- 2. Complete the card layout tray wiring charts, and release drawings of all circuits.**
- 3. Build and test the engineering model.**
- 4. Write the final reports on all circuits.**
- 5. Procure all parts and start building cards.**
- 6. Procure or design power supplies.**

6.2 Mechanical Design

Complete the mechanical design.

Section 7

KEY TECHNICAL PERSONNEL

J. G. PUENTE received a B.E.E. from Brooklyn Polytechnic Institute and an M.S.E.E. from Stevens Institute of Technology. He is a Staff Engineer in the Propagation Engineering Department of the Communications Systems Center.

Mr. Puente joined IBM in July, 1961 and was assigned to make an analysis and evaluation of a 2400 band phase reversal modem. He was previously employed at ITT Laboratories, Stavid Engineering, and Bell Telephone Laboratories. His work at these locations has been primarily in the design and development of circuits for radar equipments. The circuits he designed included RF amplifiers, mixers, modulators and circuits for precision analog to digital conversion in an FM radar. He also made design contributions in Projects Regulus, Plato and Lobar—all radar systems.

Mr. Puente has spent an average of 30 hours a week on the modulator-demodulator since 16 October 1961.

R. A. WATERS joined IBM in August, 1960 on graduating from the University of Florida with a B.E.E. degree. He is currently employed as a junior engineer in the Propagation Engineering Department of the Communications Systems Center.

On joining IBM, Mr. Waters received training as a computer programmer. Thereafter, he worked in the Systems Analysis Group of the Communications Systems Center in the role of programmer and junior engineer. In that department, Mr. Waters participated in engineering studies concerning the technical and economic characteristics of communications systems to serve the military and civil branches of the government.

He evaluated alternative methods of communications, prepared cost studies, and developed methods of integrating communications and data processing systems. In this connection, Mr. Waters worked on the Social Security Administration proposal, the Defense Communications Agency simulation proposal, and the Society of International Air Transportation Carrier proposal. He joined the Propagation Engineering Department in September, 1961.

Mr. Waters has been working approximately 40 hours a week on this job since 6 November 1961.

H. N. LEIGHTON is a Laboratory Technical Specialist in the Communications Systems Center, Propagation Engineering Department. He joined IBM in November, 1961.

Mr. Leighton graduated from Montgomery Junior College in 1951, and received a Certificate in Technical Electricity. He is currently in his sophomore year of the B.E.E. curriculum at George Washington University as a part-time student.

Mr. Leighton worked for the National Security Agency for two and one-half years, installing and repairing teletype and associated electronic equipment. He spent eight years in the Research and Engineering Laboratory of Jansky and Bailey. As an Associate Engineer he evaluated, designed, and manufactured special equipment, such as broadband receivers, automatic test sets, self-tuning transmitters, special audio and video amplifiers, and automatic photographic equipment.

Mr. Leighton has spent approximately 40 hours a week on the modulator-demodulator task since 6 November 1961.

Section 8
ABSTRACT CARDS (ASTIA)

AD _____	Accession No. _____	AD _____	Accession No. _____	Unclassified
International Business Machines Corporation, Rockville, Md. Improved Phase Modulator-Demodulator—M. George	1. Improved Phase Modulator-Demodulator 2. Signal Corps Contract DA-36-039-sc-87248 Second Quarterly Progress Report, 1 September 1961 to 30 November 1961, 18 pp 9 illus. Signal Corps (ASRDL) Contract DA 36-039-sc-87248; Technical Requirement SC1-4269 Unclassified Report	1. Improved Phase Modulator-Demodulator 2. Signal Corps Contract DA 36-039-sc-87248; Second Quarterly Progress Report, 1 September 1961 to 30 November 1961, 18 pp 9 illus. Signal Corps (ASRDL) Contract DA 36-039-sc-87248; Technical Requirement SC1-4269 Unclassified Report	1. Improved Phase Modulator-Demodulator 2. Signal Corps Contract DA 36-039-sc-87248 Second Quarterly Progress Report, 1 September 1961 to 30 November 1961, 18 pp 9 illus. Signal Corps (ASRDL) Contract DA 36-039-sc-87248; Technical Requirement SC1-4269 Unclassified Report	In conformance with objectives of the contract, this report reflects accomplishment during the report period. Progress made in the design of a modulator-demodulator is described. Logic, circuit, and mechanical designs of the units are covered in detail. The sync bit problem is described and its solution discussed. The question of the reliability of basic circuits at O/C may cause problems. Details of this problem are discussed. Brief biographies sketch the background of technical personnel having close association with the project.
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Section 9

DISTRIBUTION LIST

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CONTRACT NO. DA 36-039 SC-87248

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